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☐ 1. Document ID: US 6243857 B1

L8: Entry 1 of 6 File: USPT Jun 5, 2001

US-PAT-NO: 6243857
DOCUMENT-IDENTIFIER: US 6243857 B1

TITLE: Windows-based flowcharting and code generation system

DATE-ISSUED: June 5, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Logan, III; Frank G.	Ann Arbor	MI		
Bunch; Kenneth W.	Newport News	VA		
Davis; Teddy Martin	Norfolk	VA		
Achesinski; Jeffrey M.	Virginia Beach	VA		

US-CL-CURRENT: 717/111; 717/113, 717/125

ABSTRACT:

A machine control system (130) includes a computer (132) that generates, edits and displays a continuous multi-block flowchart representing a program and compiles the program from the flowchart to control the operations of a machine (140). The system (130) also includes a debugger (146) for displaying the flowchart in a debugger window (170) for runtime execution control of the program.

18 Claims, 11 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 9

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 2. Document ID: US 5905669 A

L8: Entry 2 of 6 File: USPT May 18, 1999

US-PAT-NO: 5905669
DOCUMENT-IDENTIFIER: US 5905669 A

TITLE: Hierarchical routing method to be implemented in a layout system for a semiconductor integrated circuit and medium on which the hierarchical routing program is stored

DATE-ISSUED: May 18, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Horita; Keisuke	Kawasaki			JP

US-CL-CURRENT: 365/51; 716/12

ABSTRACT:

A hierarchical routing method is implemented in a layout system for a semiconductor integrated circuit which has a repetitive circuit portion. The hierarchical routing method lays out circuit elements for the repetitive circuit portion with the repetitive circuit portion structured hierarchically, expands the layout for the hierarchically-structured repetitive circuit portion in a separate independent database, extracts information of connections from the expanded layout for the repetitive circuit portion, and then carries out routing. Therefore, a semiconductor integrated circuit having a repetitive circuit portion can be designed in a short period of time while excellent properties are ensured for the semiconductor integrated circuit.

12 Claims, 13 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 8

☐ 3. Document ID: US 5430873 A

L8: Entry 3 of 6 File: USPT Jul 4, 1995

US-PAT-NO: 5430873
DOCUMENT-IDENTIFIER: US 5430873 A

TITLE: Software design support apparatus

DATE-ISSUED: July 4, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Abe; Hiroaki	Sapporo			JP
Fukao; Itaru	Sapporo			JP
Taneda; Harumi	Kawasaki			JP
Kubota; Yuji	Sapporo			JP
Arima; Yasuhiko	Sapporo			JP
Nakagawa; Naoshi	Sapporo			JP
Konno; Takeo	Sapporo			JP
Arihara; Yoshinori	Sapporo			JP
Suzuki; Yuriko	Sapporo			JP

US-CL-CURRENT: 717/113; 707/102

ABSTRACT:

During a software designing operation, a designer accesses a level prescribing unit through an interaction managing control unit. The level prescribing unit provides the guidance to specification information and design parts, etc. at a desired design level. If the designer selects and inputs specification information or design parts, the design editor corresponding to the design specification information in a design editor unit is activated, so that the designer is guided and aided through a display to produce a desired software. At this time, the information about the state of the editing operation "completed" or "not completed" is stored with the directory. The designed document satisfying a specific condition, for example, a document determined to be "design completed", is stored as a data base by a design data base storing unit. To update the information stored in the design data base, a design information inconsistency correction support unit presents the designer with the part of the information affected by the update, thereby supporting the correction.

36 Claims, 50 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 50

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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☐ 4. Document ID: US 5235702 A

L8: Entry 4 of 6 File: USPT Aug 10, 1993

US-PAT-NO: 5235702
DOCUMENT-IDENTIFIER: US 5235702 A

TITLE: Automated posting of medical insurance claims

DATE-ISSUED: August 10, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Miller; Brent G.	Toledo	OH	43613	

US-CL-CURRENT: 707/102; 705/2, 705/4, 707/101

ABSTRACT:

A method for inputting into a computerized data base system data disposed in a known format and comprising machine generated text is disclosed. The method comprises the steps of providing a document of known format; inputting the document into a computer system and converting the document into computer readable characters without manual typing of each characters; reconstructing within the computer the converted text which does not conform to the known format; flagging converted text which does not conform to the known format and which cannot be reconstructed; manually correcting the flagged text; and inputting the converted document to a computerized data base system.

30 Claims, 16 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 16

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

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☐ 5. Document ID: US 5197016 A

L8: Entry 5 of 6 File: USPT Mar 23, 1993

US-PAT-NO: 5197016
DOCUMENT-IDENTIFIER: US 5197016 A

TITLE: Integrated silicon-software compiler

DATE-ISSUED: March 23, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Sugimoto; Tai	Columbia	SC		
Kobayashi; Hideaki	Columbia	SC		
Shindo; Masahiro	Osaka			JP
Nakayama; Haruo	Osaka			JP

US-CL-CURRENT: 716/8; 716/11, 716/12, 716/17, 716/18

ABSTRACT:

A computer-aided system and method is disclosed for designing an application specific integrated circuit (ASIC) whose intended function is implemented both by a hardware subsystem including hardware elements on the integrated circuit and by a software subsystem including a general purpose microprocessor also on the integrated circuit. The system also generates software instructions for use by the software subsystem. The system utilizes a knowledge based expert system, with a knowledge base extracted from expert ASIC designers, and thus makes it possible for ASIC's to be designed and provided quickly and economically by persons not having the highly specialized skill of an ASIC designer.

32 Claims, 7 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 7

☐ 6. Document ID: US 4922432 A

L8: Entry 6 of 6 File: USPT May 1, 1990

US-PAT-NO: 4922432
DOCUMENT-IDENTIFIER: US 4922432 A

TITLE: Knowledge based method and apparatus for designing integrated circuits using functional specifications

DATE-ISSUED: May 1, 1990

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kobayashi; Hideaki	Columbia	SC		
Shindo; Masahiro	Osaka			JP

US-CL-CURRENT: 716/17; 345/441

ABSTRACT:

The present invention provides a computer-aided design system and method for designing an application specific integrated circuit which enables a user to define functional architecture independent specifications for the integrated circuit and which translates the functional architecture independent specifications into the detailed information needed for directly producing the integrated circuit. The functional architecture independent specifications of the desired integrated circuit can be defined at the functional architecture independent level in a flowchart format. From the flowchart, the system and method uses artificial intelligence and expert systems technology to generate a system controller, to select the necessary integrated circuit hardware cells needed to achieve the functional specifications, and to generate data and control paths for operation of the integrated circuit. This list of hardware cells and their interconnection requirements is set forth in a netlist. From the netlist it is possible using known manual techniques or existing VLSI CAD layout systems to generate the detailed chip level topological information (mask data) required to produce the particular application specific integrated circuit.

20 Claims, 17 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 12

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